

*Amendments to the Claims*

The listing of claims will replace all prior versions, and listings of claims in the application.

1. *(currently amended)* An ESD protection circuit, comprising:

one or more first diodes on a first area of P-substrate coupled in series between a supply voltage and a terminal pad;

a second diode on said first area of P-substrate coupled to a ground, said second diode having an n+ region; and

one or more third diodes on a second area of P-substrate coupled in series between said terminal pad and said second diode, each of said one or more third diodes having a deep N-well that separates said second area of P-substrate from said first area of P-substrate ~~wherein said one or more third diodes are configured to enable a voltage on an interconnection node between said one or more third diodes and said second diode that is different from ground;~~

~~wherein said ESD protection circuit increases the allowable signal swing at said terminal pad.~~

2. *(currently amended)* The ESD protection circuit of claim 1, wherein said one or more third diodes each includes an n+ region on an said second area of P-substrate surrounded by a said deep N-well.

3. *(currently amended)* The ESD protection circuit of claim [[2]]1, wherein said deep N-well ~~separates said area of P-substrate from a common area of P-substrate~~

isolates a voltage on an interconnection node between said one or more third diodes and said second diode from said ground.

4. (currently amended) The ESD protection circuit of claim ~~[[3]]~~1, wherein said ~~common~~ first area of P-substrate is coupled to said ground.

5. (currently amended) The ESD protection circuit of claim 1, wherein ~~said~~ an allowable signal swing at said terminal pad is greater than said supply voltage plus 1.4 V.

6. (currently amended) The ESD protection circuit of claim 1, wherein a forward turn-on voltage of each of said one or more first diodes, said second diode, and said one or more third diodes is approximately 0.7 V.

7. (currently amended) An ESD protection circuit, comprising:

one or more ~~of a~~ first diodes on a first area of P-substrate coupled in series between a supply voltage and a terminal pad, each of said one or more first diodes having a p+ region in an N-well;

a second diode on said first area of P-substrate coupled to a ground, said second diode having an n+ region; and

one or more ~~of a~~ third diodes on a second area of P-substrate coupled in series between said terminal pad and said second diode, ~~wherein~~ each of said one or more third diodes ~~includes~~ having an n+ region on an said second area of P-substrate separated by a deep N-well from a ~~common~~ said first area of P-substrate;

~~wherein said ESD protection circuit increases the allowable signal swing at said terminal pad.~~

8. *(canceled)*

9. *(canceled)*

10. *(currently amended)* The ESD protection circuit of claim 7, wherein said ~~common~~ first area of P-substrate is coupled to said ground.

11. *(currently amended)* The ESD protection circuit of claim 7, wherein said ~~an~~ an allowable signal swing at said terminal pad is greater than said supply voltage plus 1.4 V.

12. *(currently amended)* The ESD protection circuit of claim 7, wherein a forward turn-on voltage of each of said one or more first diodes, said second diode, and said one or more third diodes is approximately 0.7 V.

13. *(currently amended)* An ESD protection circuit, comprising:

a first diode on a first area of P-substrate having a cathode coupled to a supply voltage and an anode coupled to a cathode of a second diode, said second diode on said first area of P-substrate having an anode coupled to a terminal pad; and

a third diode on a second area of P-substrate having a cathode coupled to said terminal pad and an anode coupled to a cathode of a fourth diode, said fourth diode on

said first area of P-substrate having an anode coupled to a ground, wherein said third diode includes an n+ region on an said second area of P-substrate separated by a deep N-well from ~~a common~~ said first area of P-substrate, and wherein said fourth diode includes an n+ region on said first area of P-substrate;

~~wherein said ESD protection circuit increases the allowable signal swing at said terminal pad.~~

14. *(currently amended)* The ESD protection circuit of claim 13, wherein said first diode and said second diode each includes an n+ region in an N-well on said ~~common~~ first area of P-substrate.

15. *(currently amended)* The ESD protection circuit of claim 13, wherein ~~said fourth diode includes an n+ on said common area of P-substrate~~ an interconnection node between said third diode and said fourth diode is isolated from said ground.

16. *(currently amended)* The ESD protection circuit of claim 13, wherein said ~~common~~ first area of P-substrate is coupled to said ground.

17. *(currently amended)* The ESD protection circuit of claim 13, wherein ~~said~~ an allowable signal swing at said terminal pad is greater than said supply voltage plus 1.4 V.

18.     *(currently amended)* The ESD protection circuit of claim 13, wherein a forward turn-on voltage of each of said first diode, said second diode, said third diode, and said fourth diode is approximately 0.7 V.